

2/11 AUS920030766US1

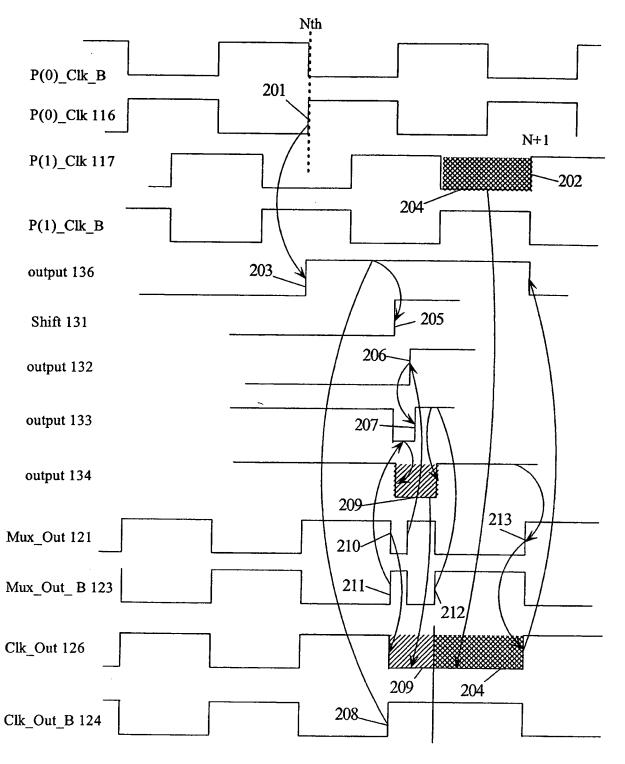


FIG. 2

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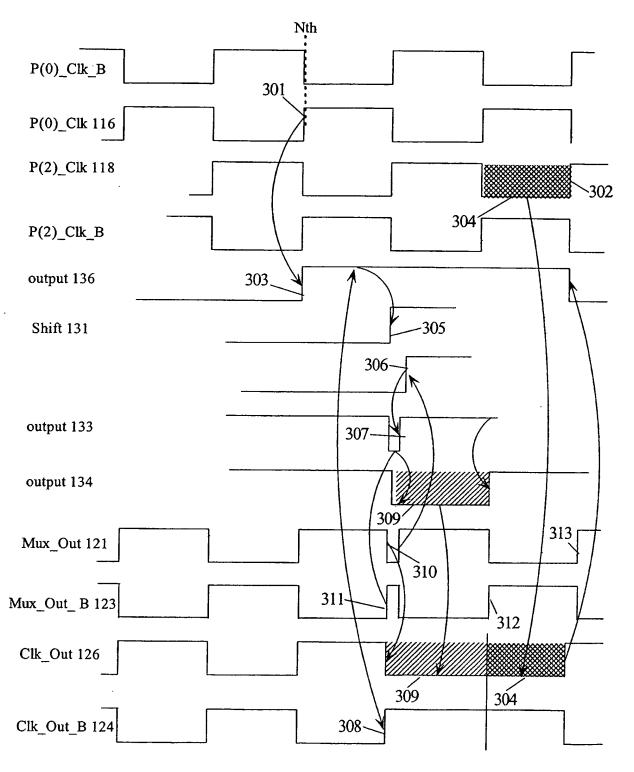


FIG. 3

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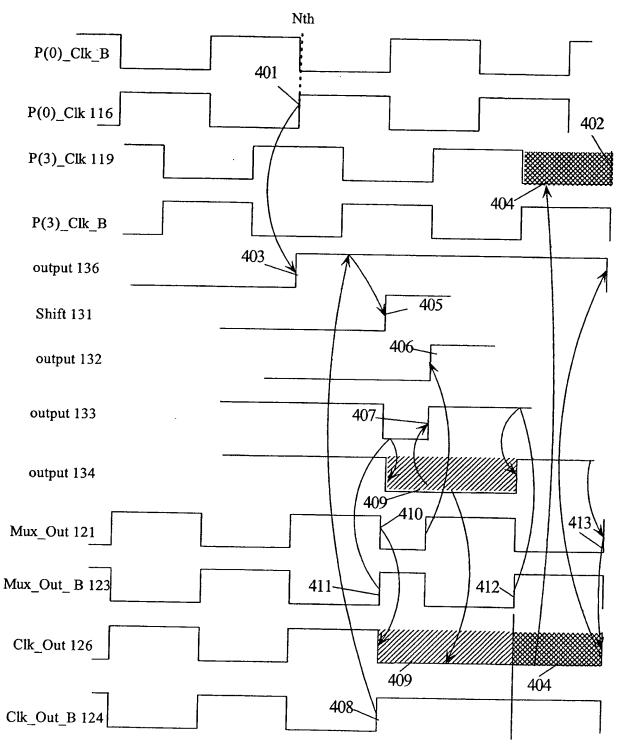
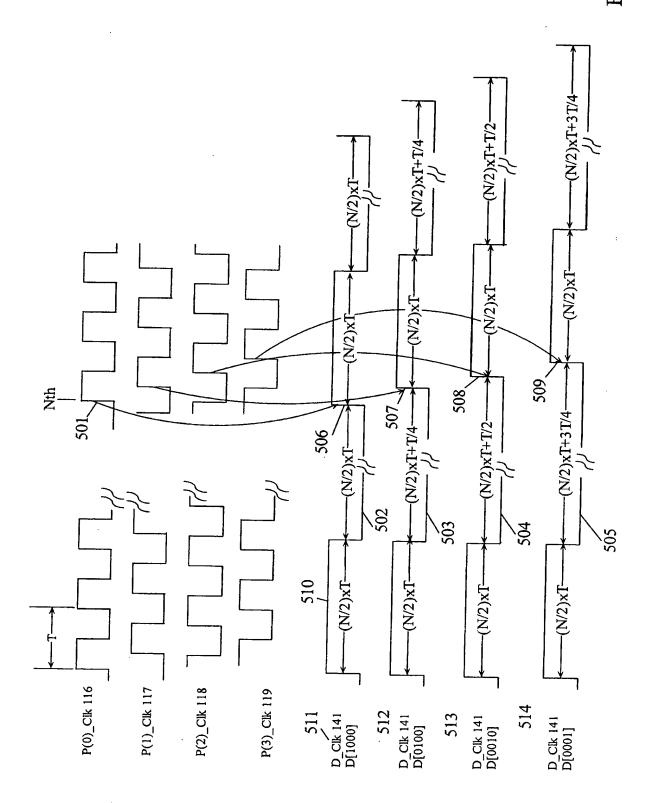


FIG. 4

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601 602	60.	3	604	60:	5 112	113	114	115
Number of N cycles	R₀	R ₁	R ₂	R ₃	P_SEL(0)	P_SEL(1)	P_SEL(2)	P_SEL(3)
0	R ₀	R ₁	R ₂	R ₃	1	0	0	0
1	R₀	R ₁	R ₂	R ₃	1	0	0	0
2	Ro	R ₁	R ₂	R ₃	1	0	0	0
•	R _o	R₁	R ₂	R ₃	1	0	0	0
n	R₀	R ₁	R ₂	R ₃	1	0	0	0

Decoder output 135 = D [1000]

FIG. 6A

601 602	603	3 <i>E</i>	04	6(05	2 113	114	115
Number of N cycles	R₀	R₁	R ₂	R ₃	P_SEL(0)	P_SEL(1)	P_SEL(2)	P_SEL(3)
0	R₀	R ₁	R ₂	R ₃	1	0	0	0
1	R ₃	R_0	R ₁	R ₂	0	1	0	0
2	R ₂	R ₃	R ₀	R₁	0	0	1	0
3	R ₁	R ₂	R ₃	R₀	0	0	0	1
4	R_0	R ₁	R ₂	R ₃	1	0	0	0

Decoder output 135 = D [0100]

FIG. 6B

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601 602	2 ()3	604	6	05	2 113	114	115
Number of N cycles	R_0	R ₁	R ₂	R ₃	P_SEL(0)	P_SEL(1)	P_SEL(2)	P_SEL(3)
0	Ro	R₁	R ₂	R ₃	1	0	0	0
1	R ₂	R ₃	R ₀	R ₁	0	0	1	0
2	R₀	R₁	R ₂	R ₃	1	0	0	0
3	R ₂	R ₃	R _o	R ₁	0	0	1	0
4	Ro	R ₁	R ₂	R ₃	1	0	0	0

Decode [0010]

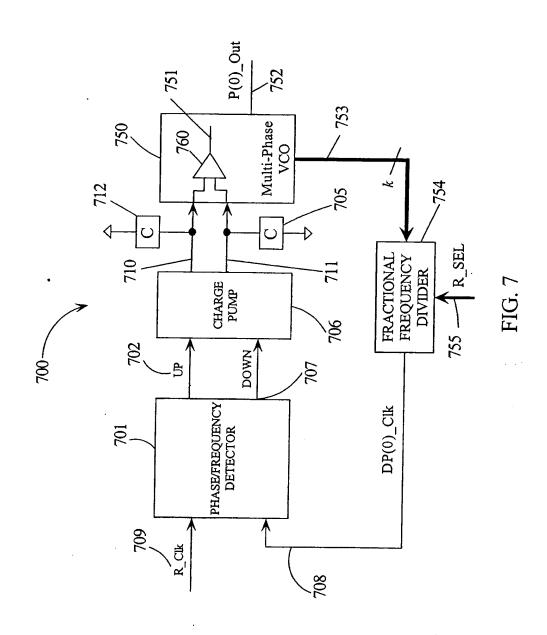
FIG. 6C

601 602	60	3 (604	60	112	113	114	115
Number of N cycles	Ro	R ₁	R ₂	R_3	P_SEL(0)	P_SEL(1)	P_SEL(2)	P_SEL(3)
0	Ro	R ₁	R ₂	R ₃	1	0	0	0
1	R₁	R ₂	R ₃	Ro	0	0	0	1
2	R ₂	R ₃	R _o	R₁	0	0	1	0
3	R ₃	R _o	R ₁	R ₂	0	1	0	0
4	R ₀	R₁	R ₂	R ₃	1	0	0	0

Decode [0001]

FIG. 6D

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9/11 AUS920030788US1 834 838 COMMUNICATIONS ADAPTER NETWORK DISPLAY ADAPTER 818 I/O ADAPTER 832 828 820 RAM 814 822 USER INTERFACE ADAPTER 826 816 ROM 810 824 CPU

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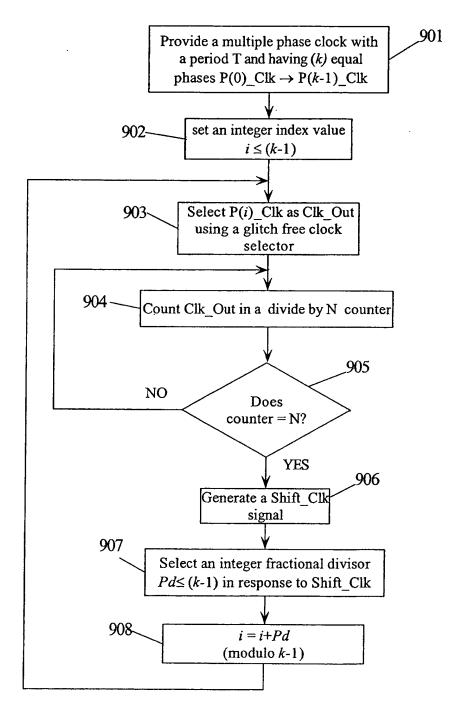


FIG. 9

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